ABSTRACT OF THE DISCLOSURE

An integrated circuit arrangement which has vertical FET selection transistors and storage capacitors in each case of a transistor array and of an assigned memory cell array, said storage capacitors being formed vertically into the depth of a substrate in deep trenches a test structure is integrated, which enables a plurality of vertical FET selection transistors with one another by a conductive electrode material embedded in an extended deep trench With a test structure of this type, it is possible to evaluate characteristic values for leakage currents and capacitances at different semiconductor junctions and also between different sections of the integrated circuit arrangement and also to perform reliability stress tests.

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